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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,550	06/27/2003	Edward A. Burton	INTEL-021	7414

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EXAMINER	
TRAN, LONG K	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/607,550	EDWARD A. BURTON	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amdt on March 14, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3 – 5, 7 – 14, 29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 – 5, 7 – 14, 29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on March 14, 2005.

2. Claims **2, 6** and **15 – 28** have been cancelled.

3. Claims **1, 3, 7, 11** and **29** have been amended.

4. Claims **1, 3 – 5, 7 – 14, 29** and **30** are presented for examination.

5. The examiner has withdrawn the examiner's statement of reasons for the indication of allowable subject matter in the previous Non-Final Office Action mailed on January 31, 2005.

Drawings

6. The drawings were received on March 14, 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **1, 3, 7, 8, 10, 11** and **12** are rejected under 35 U.S.C. 102(b) as being anticipated by Otsuka (US Patent no. 6,275,407).

9. Regarding claim **1**, the patent 407 illustrates a semiconductor device, comprising:

a first layer having a plurality of signal wires SENSE PAIR LINE (figs. 6 and 10B; col. 11, lines 11 – 383); and

a second layer adjacent to the first layer having a plurality of signal wires DATA PAIR LINE (figs. 6 and 10B; col. 11, lines 11 – 38), wherein the signal wires in the first

laver are substantially parallel with the signal wires in the second laver (figs. 6 and 10B; col. 8, lines 20 23 and col. 11, lines 11 – 38) and wherein adjacent signal wires are located in an alternating pattern in the first and second layers (fig. 6 and 10B; col. 8, lines 20 – 23 and col. 11, lines 11 – 38).

Regarding claim **3**, the patent 407 illustrates the alternating pattern has every other signal wire residing in the same layer (fig. 6 and 10B; col. 8, lines 20 – 23 and col. 11, lines 11 – 38).

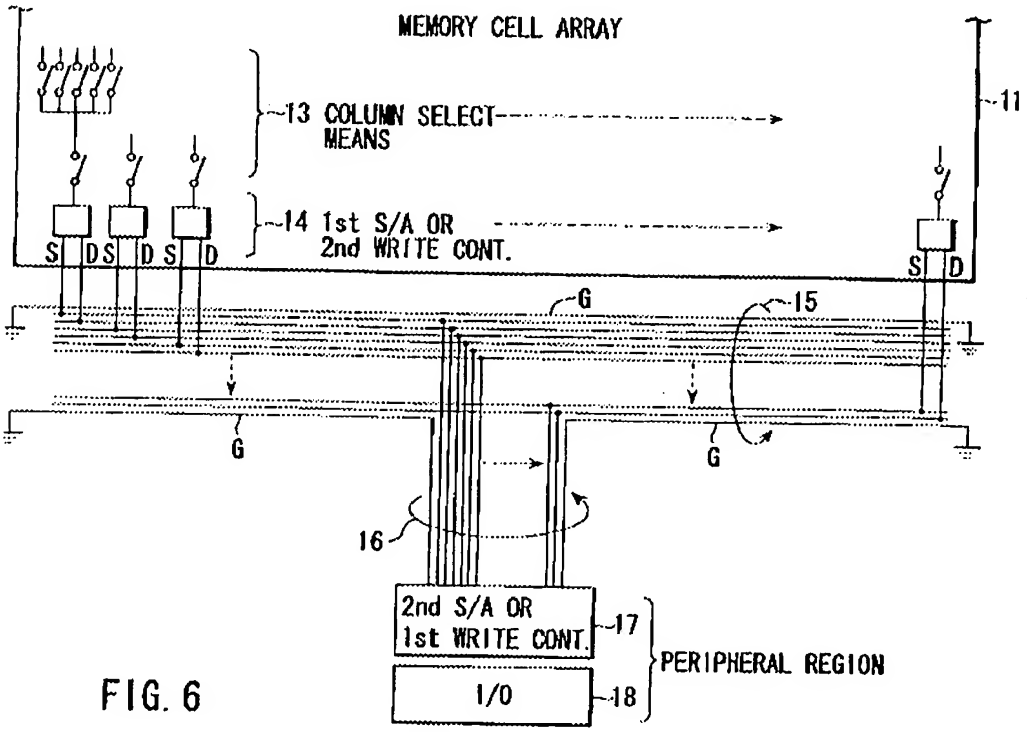


FIG. 6

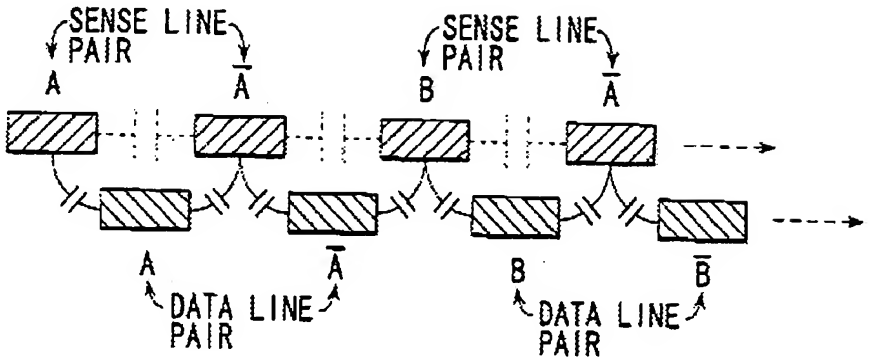


FIG. 10B

10. Regarding claim **7**, the patent 407 illustrates a semiconductor device, comprising:

a first layer having a plurality of signal wires SENSE PAIR LINE (figs. 6 and 10B; col. 11, lines 18 – 38); and

a second layer adjacent to the first layer having a plurality of signal wires DATA PAIR LINE (figs. 6 and 10B; col. 11, lines 18 – 38), wherein the signal wires in the first laver are substantially parallel with the signal wires in the second laver (figs. 6 and 10B; col. 8, lines 20 23 and col. 11, lines 11 – 38); and

at least one additional layer S or D (fig. 6. Note: there are more than one SENSE PAIR LINE layer (S) and DATA PAIR LINE layer (D) that are parallel to each other in fig. 6; and they are identical to the SENSE PAIR LINE layer and DATA PAIR LINE layer in fig. 10B) adjacent to the first and second layer , wherein adjacent signal wires are located in an alternating pattern in the first and second layers (fig. 6 and 10B; col. 8, lines 20 – 23 and col. 11, lines 11 – 38).

Regarding claim **8**, the patent 407 illustrates N layers ("As a matter of course, a plurality of the sense line pairs and the data line pairs, the number of which are the same are disposed similarly. In the foregoing case, the number of the sense line pairs and that of the data line pairs are the same. Therefore, all of the sense line pairs and the data line pairs can completely be disposed in parallel with each other" (col. 9, lines 6 – 13)), wherein N is greater than two and wherein the first and second layers are any two adjacent layers in the N layers.

Regarding claim **10**, the patent 407 illustrates the first and second layers having similar process parameters (col. 9, lines 6 – 13). Note: However this limitation is taken to be a product by process limitation, it is the patentability product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections ***102 or 103*** is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim **11**, the patent 407 illustrates the pluralities of signal wires SENSE PAIR LINES and DATA PAIR LINES in the first and second layer are a first set of signal wires configured to carry a first set of related signals (fig. 6).

Regarding claim **12**, the patent 407 illustrates the second set of signal wires being replicated in the first and second layers (fig. 6).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

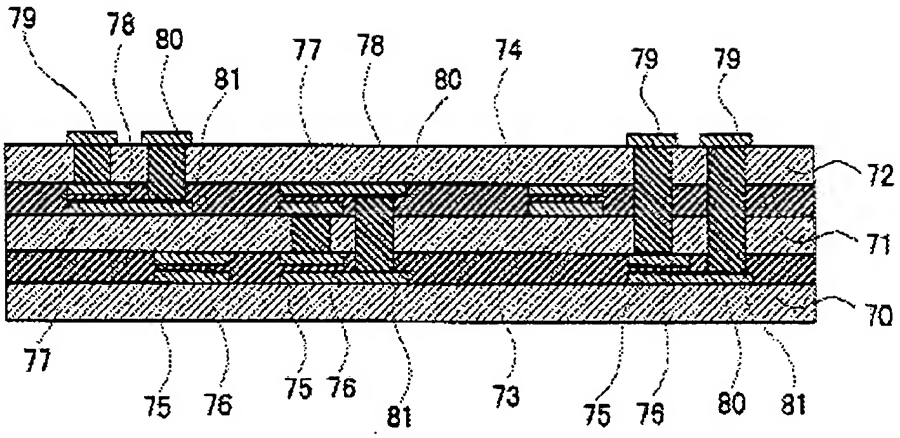
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims **1, 8, 9, 10, 13, 14, 29** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka et al. (US Patent 6,476,330) in view of Otsuka (US Patent no. 6,275,407).

13. Regarding claim **1**, the patent 330 illustrates a semiconductor device comprising:

A first layer (not shown same as 35 (fig. 4D)) having a plurality of signal wires 75 (fig. 8), a second layer (not shown same as 38 (fig. 4D)) adjacent to the first layer having a plurality of signal wires 76 (fig. 8), wherein the signal wires in the first and second layers are substantially parallel with each other (column 9, lines 45 – 47).

FIG. 8



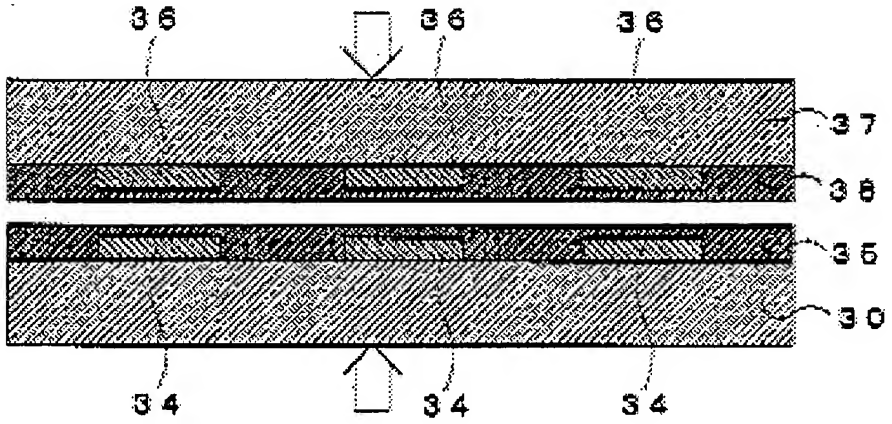


FIG. 4D

The patent 330 does not show the adjacent signal wires are located in an alternating pattern in the first and second pattern.

However, the patent 407 shows the adjacent signal wires are located in an alternating pattern in the first and second layers (fig. 6 and 10B; col. 8, lines 20 – 23 and col. 11, lines 11 – 38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the adjacent signal wires of the 330's device with the

adjacent signal wires being located in an alternating pattern in the first and second layers of 407's device, in order to have a structure that the signal line width of each of the sense lines and the data lines being enlarged to reduce the wiring resistance (col. 11, lines 39 – 41).

Regarding claim **8**, the patent 330 illustrates the semiconductor device comprising: N layers, wherein **N** is greater than two and wherein the first and second layers are any adjacent layers in the **N** layers (fig. 8).

Regarding claim **9**, the patent 330 illustrates the semiconductor device is a microprocessor (column 1, lines 6 – 15).

Regarding claim **10**, the patent 330 illustrates the first layer and second layer have similar process parameters (column 11, lines 25+). Note: However this limitation is taken to be a product by process limitation, it is the patentability product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections ***102 or 103*** is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old

or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim **13**, the patent 330 illustrates additional signal wires in the second layer that are located substantially orthogonal to the plurality of signal wires in the first layer (note: column 11, lines31 – 34: the first and second signal wires can run in any direction. Therefore they can run parallel or orthogonally).

Regarding claim **14**, the patent 330 illustrates the plurality of signal wires in the first layer is a set of related signal wires and wherein the plurality of signal wires in the second layer is a replication of the plurality of signal wires in the first layer (fig. 8).

14. Regarding claim **29**, the patent 330 illustrates a system comprising a microprocessor; and off-die component in communication with the microprocessor; wherein the microprocessor (column 1; 5 +) comprising:

A first layer (not shown same as 35 (fig. 4)) having a plurality of signal wires 75 (fig. 8), a second layer (not shown same as 38 (fig. 4)) adjacent to the first layer having a plurality of signal wires 76 (fig. 8), wherein the signal wires in the first and second layers are substantially parallel with each other (column 9, lines 45 – 47).

The patent 330 does not show the adjacent signal wires are located in an alternating pattern in the first and second pattern.

However, the patent 407 shows the adjacent signal wires are located in an alternating pattern in the first and second layers (fig. 6 and 10B; col. 8, lines 20 – 23 and col. 11, lines 11 – 38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the adjacent signal wires of the 330's device with the adjacent signal wires being located in an alternating pattern in the first and second layers of 407's device, in order to have a structure that the signal line width of each of the sense lines and the data lines being enlarged to reduce the wiring resistance (col. 11, lines 39 – 41).

Regarding claim **30**, the patent 330 illustrates at least one additional layer adjacent to the first and second layer (not shown same as 35 (fig. 4)), wherein signal wires 77 (fig. 8) in the at least one additional layer are substantially parallel to signal wires in the first and second layers.

15. Claims **4** and **5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka et al. (US Patent 6,476,330) in view of Otsuka (US Patent no. 6,275,407) and further in view of Schaper (US Patent No. 6,388,200).

16. Regarding claim **4**, the patents 330 and 407 illustrate the claimed invention of claim 1 except for a power supply and ground wires are located in both the first layer and the second layer as cited in present claim.

However, Schaper shows in figure 1 that power connection 26 in layer 15 and power pad 21 in layer 17; ground pad 20 in layer 17 and ground connection 24 in layer 15.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the signal wire layers of the 330's and 407's devices with

the signal wires layers of Shaper, in order to interconnect different signal wires to the power and ground source in a four metal layer structure.

Regarding claim **5**, figure 1 of Schaper illustrates power supply and ground wires are located in the same respective position in each layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LKT

May 2, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Amendments to the Drawings

The attachments to this paper include replacement sheets for Figures 1 and 2, which provide a legend for each of these drawings.

OK to enter /MF/ 4/26/05